said wiring substrate having a number of through-holes;

a number of bumps formed respectively in said through-holes in conforming relationship with said two or more chip electrodes and electrically connecting said wiring with said two or more chip electrodes; and

an external bump pad electrically connected through said common wiring layer to said two or more chip electrodes.

22. A semiconductor device comprising:

a wiring substrate having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on the other surface of said wiring substrate and having two or more chip electrodes in a common wiring layer, wherein said chip electrodes are arranged parallel to an edge of said semiconductor chip and said wiring is bent at at least one position;

said wiring substrate having a number of through-holes;

a number of bumps formed respectively in said through-holes in conforming relationship with said two or more chip electrodes and electrically connecting said wiring with said two or more chip electrodes; and

an external bump pad electrically connected through said common wiring layer to said two or more chip electrodes.

23. A semiconductor device comprising:

a wiring substrate having a predetermined pattern of wiring formed on one surface;

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a semiconductor chip disposed on the other surface of said wiring substrate and having two or more chip electrodes in a common wiring layer, wherein said chip electrodes are arranged parallel to an edge of said semiconductor chip and said wiring has an end width larger than an inter-electrode distance between said chip electrodes;

said wiring substrate having a number of through-holes;

a number of bumps formed respectively in said through-holes in conforming relationship with said two or more chip electrodes and electrically connecting said wiring with said two or more chip electrodes; and

an external bump pad electrically connected through said common wiring layer to said two or more chip electrodes.

24. A semiconductor device according to claim 21, wherein said chip electrodes comprise at least one kind of terminals selected from ground, power-source and signal terminals of said semiconductor chip.

25. A semiconductor device according to claim 22, wherein said chip electrodes comprise at least one kind of terminals selected from ground, power-source and signal terminals of said semiconductor chip.

26. A semiconductor device according to claim 23, wherein said chip electrodes comprise at least one kind of terminals selected from ground, power-source and signal terminals of said semiconductor chip.

27. A semiconductor device comprising:

a wiring substrate having a predetermined pattern of wiring formed on one surface;

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a semiconductor chip disposed on said one surface of said wiring substrate and having two or more chip electrodes in a common wiring layer, wherein said chip electrodes are arranged from an edge of said semiconductor chip toward its inner side;

a number of bumps disposed on said wiring respectively in conforming relationship with said two or more chip electrodes and electrically connecting said wiring with said two or more chip electrodes; and

an external pump pad electrically connected through said common wiring layer to said two or more chip electrodes.

28. A semiconductor device comprising:

a wiring substrate having a predetermined pattern of working formed on one surface;

a semiconductor chip disposed on said one surface of said wiring substrate and having two or more chip electrodes in a common wiring layer, wherein said chip electrodes are arranged parallel to an edge of said semiconductor chip and said wiring is bent at at least one position;

a number of bumps disposed on said wiring respectively in conforming relationship with said two or more chip electrodes and electrically connecting said wiring with said two or more chip electrodes; and

an external bump pad electrically connected through said common wiring layer to said two or more chip electrodes.

29. A semiconductor device comprising:

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a wiring substrate having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on said one surface of said wiring substrate and having two or more chip electrodes in a common wiring layer, wherein said chip electrodes are arranged parallel to an edge of said semiconductor chip and said wiring has an end width larger than an inter-electrode distance between said chip electrodes;

a number of bumps disposed on said wiring respectively in confirming relationship with said two or more chip electrodes and electrically connecting said wiring with said two or more chip electrodes; and

an external bump pad electrically connected through said common wiring layer to said two or more chip electrodes.

30. A semiconductor device according to claim 27, wherein said chip electrodes comprise at least one kind of terminals selected from ground, power-source and signal terminals of said semiconductor chip.

31. A semiconductor device according to claim 28, wherein said chip electrodes comprise at least one kind of terminals selected from ground, power-source and signal terminals of said semiconductor chip.

32. A semiconductor device according to claim 29, wherein said chip electrodes comprise at least one kind of terminals selected from ground, power-source and signal terminals of said semiconductor chip.

33. A semiconductor device comprising:

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a TAB (tape automated bonding) tape having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on the other surface of said TAB tape and having two or more chip electrodes in a common wiring layer, wherein said chip electrodes are arranged from an edge of said semiconductor chip toward its inner side;

said TAB tape having a number of through-holes;

a number of bumps formed respectively in said through-holes in conforming relationship with said two or more chip electrodes and electrically connecting said wiring with said two or more chip electrodes; and

an external bump pad electrically connected through said common wiring layer to said two or more chip electrodes.

34. A semiconductor device comprising:

a TAB (tape automated bonding) tape having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on the other surface of said TAB tape and having two or more chip electrodes in a common wiring layer, wherein said chip electrodes are arranged parallel to an edge of said semiconductor chip and said wiring is bent at at least one position;

said TAB tape having a number of through-holes;

a number of bumps formed respectively in said through-holes in conforming relationship with said two or more chip electrodes and electrically connecting said wiring with said two or more chip electrodes; and

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an external bump pad electrically connected through said common wiring layer to said two or more chip electrodes.

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35. A semiconductor device comprising:

a TAB (tape automated bonding) tape having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on the other surface of said TAB tape and having two or more chip electrodes in a common wiring layer, wherein said chip electrodes are arranged parallel to an edge of said semiconductor chip and said wiring has an end width larger than an inter-electrode distance between said chip electrodes;

said TAB tape having a number of through-holes;

a number of bumps formed respectively in said through-holes in conforming relationship with said two or more chip electrodes and electrically connecting said wiring with said two or more chip electrodes; and

an external bump pad electrically connected through said common wiring layer to said two or more chip electrodes.

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36. A semiconductor device according to claim 33, wherein said chip electrodes comprise at least one kind of terminals selected from ground, power-source and signal terminals of said semiconductor chip.

37. A semiconductor device according to claim 34, wherein said chip electrodes comprise at least one kind of terminals selected from ground, power-source and signal terminals of said semiconductor chip.

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38. A semiconductor device according to claim 35, wherein said chip electrodes comprise at least one kind of terminals selected from ground, power-source and signal terminals of said semiconductor chip.

39. A semiconductor device comprising:

a TAB tape having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on said one surface of said TAB tape and having two or more chip electrodes in a common wiring layer, wherein said chip electrodes are arranged from an edge of said semiconductor chip toward its inner side;

a number of bumps disposed on said wiring respectively in conforming relationship with said two or more chip electrodes and electrically connecting said wiring with said two or more chip electrodes; and

an external bump pad electrically connected through said common wiring layer to said two or more chip electrodes.

40. A semiconductor device comprising:

a TAB tape having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on said one surface of said TAB tape and having two or more chip electrodes in a common wiring layer, wherein said chip electrodes are arranged parallel to an edge of said semiconductor chip and said wiring is bent at at least one position;

a number of bumps disposed on said wiring respectively in conforming relationship with said two or more chip electrodes and electrically connecting said wiring with said two or more chip electrodes; and

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an external bump pad electrically connected through said common wiring layer to said two or more chip electrodes.

41. A semiconductor device comprising:

a TAB tape having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on said one surface of said TAB tape and having two or more chip electrodes in a common wiring layer, wherein said chip electrodes are arranged parallel to an edge of said semiconductor chip and said wiring has an end width larger than an inter-electrode distance between said chip electrodes;

a number of bumps disposed on said wiring respectively in conforming relationship with said two or more chip electrodes and electrically connecting said wiring with said two or more chip electrodes; and

an external bump pad electrically connected through said common wiring layer to said two or more chip electrodes.

42. A semiconductor device according to claim 39, wherein said chip electrodes comprise at least one kind of terminals selected from ground, power-source and signal terminals of said semiconductor chip.

43. A semiconductor device according to claim 40, wherein said chip electrodes comprise at least one kind of terminals selected from ground, power-source and signal terminals of said semiconductor chip.

44. A semiconductor device according to claim 41, wherein said chip electrodes comprise at least one kind of terminals selected from ground, power-source and signal terminals of said semiconductor chip.--

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